CLAIMS

1. A method for analyzing an integrated circuit (IC), the method comprising:

measuring a first delay value from a first embedded test circuit in the IC, the first embedded test circuit comprising a first ring oscillator coupled to a first test load, the first test load being formed at least in part in a first interconnect layer in the IC;

measuring a second delay value from a second embedded test circuit in the IC, wherein the second embedded test circuit is an unloaded test circuit, the second embedded test circuit comprising a second ring oscillator, the second ring oscillator being substantially similar to the first ring oscillator; and

comparing the first delay value to the second delay value.

2. The method of Claim 1, wherein comparing the first delay value to the second delay value comprises generating a set of parameter equations, the set of parameter equations comprising:

a first parameter equation specifying a first Front End Of the Line (FEOL) parameter as a function of the first delay value and the second delay value; and

a second parameter equation specifying a first Back End Of the Line (BEOL) parameter as a function of the first delay value and the second delay value, wherein the first BEOL parameter represents a characteristic of the at least one interconnect layer.

3. The method of Claim 2, wherein generating the set of parameter equations comprises:

providing a first model equation for the first embedded test circuit, the first model equation specifying the first delay value as a function of the first FEOL parameter and the second BEOL parameter;

providing a second model equation for the second embedded test circuit, the second model equation specifying the second delay value as a function of the first FEOL parameter and the second BEOL parameter;

solving the first model equation and the second model equation for the first FEOL parameter to generate the first parameter equation; and

solving the first model equation and the second model equation for the first BEOL parameter to generate the second parameter equation.

4. The method of Claim 3, wherein the first model equation comprises a first FEOL parameter variable multiplied by a first FEOL correction factor and a first BEOL parameter variable multiplied by a first BEOL correction factor, and

wherein the second model equation comprises the first FEOL parameter variable multiplied by a second FEOL correction factor and the first BEOL parameter variable multiplied by a second BEOL correction factor.

5. The method of Claim 4, wherein the first FEOL parameter is transistor speed, and wherein the first FEOL correction factor and the second FEOL correction factor are equal to one.

6. The method of Claim 3, wherein comparing the first delay value to the second delay value further comprises:

substituting the first delay value and the second delay value into the first parameter equation to obtain an actual value for the first FEOL parameter;

comparing the actual value for the first FEOL parameter to an expected value for the first FEOL parameter;

substituting the first delay value and the second delay value into the second parameter equation to obtain an actual value for the first BEOL parameter; and

comparing the actual value for the first BEOL parameter to an expected value for the first BEOL parameter.

7. The method of Claim 1, wherein the IC is a field programmable gate array (FPGA), and

wherein measuring the first delay value comprises configuring the FPGA into a measurement circuit and reading the first delay value using the measurement circuit, and

wherein measuring the second delay value comprises configuring the FPGA into the measurement circuit and reading the second delay value using the measurement circuit.

8. The method of Claim 1, further comprising:

measuring a third delay value from a third embedded test circuit in the IC, the third embedded test circuit comprising a third ring oscillator coupled to a third test load, the third test load being formed in a second interconnect layer in the IC; and

comparing the third delay value to the first delay value and the second delay value.

9. A method for analyzing an integrated circuit (IC), the method comprising:

creating a first embedded test circuit in the IC for generating a first output delay, the first embedded test circuit comprising a first ring oscillator coupled to a first test load, the first test load being formed in a first interconnect layer of the IC;

creating a second embedded test circuit in the IC for generating a second output delay, the second embedded test circuit comprising a second ring oscillator, the second ring oscillator being an unloaded

ring oscillator, the second ring oscillator being substantially similar to the first ring oscillator;

providing a first parameter equation and a second parameter equation, the first parameter equation and the second parameter equations specifying a first Front End Of the Line (FEOL) parameter and a first Back End Of the Line (BEOL) parameter, respectively, as functions of the first output delay and the second output delay;

measuring a first measured output delay and a second measured output delay from the first embedded test circuit and the second embedded test circuit, respectively;

substituting the first measured output delay and the second measured output delay into the first parameter equation to generate a first FEOL parameter value; and

substituting the first measured output delay and the second measured output delay into the second parameter equation to generate a first BEOL parameter value.

10. The method of Claim 9, further comprising:

creating a third embedded test circuit in the IC for generating a third output delay, the third embedded test circuit comprising a third ring oscillator coupled to a second test load, the second test load being formed in a second interconnect layer of the IC, the third ring oscillator being substantially similar to the first ring oscillator;

providing a third parameter equation, the third parameter equation specifying a second BEOL parameter as a function of the second output delay and the third output delay;

measuring a third measured output delay from the third embedded test circuit;

substituting the third measured output delay into the third parameter equation to generate a second BEOL parameter value.

11. The method of Claim 9, wherein providing the first parameter equation and the second parameter equation comprises:

providing a first model equation for the first embedded test circuit, the first model equation specifying the first output delay as a function of the first FEOL parameter and the first BEOL parameter;

providing a second model equation for the second embedded test circuit, the second model equation specifying the second output delay as a function of the first FEOL parameter and the first BEOL parameter;

solving the first model equation and the second model equation for the first FEOL parameter to generate the first parameter equation; and

solving the first model equation and the second model equation for the first BEOL parameter to generate the second parameter equation.

12. The method of Claim 11, wherein providing the first parameter equation and the second parameter equation further comprises defining a first FEOL correction factor, a second FEOL correction factor, a first BEOL correction factor, and a second BEOL correction factor,

wherein the first model equation comprises a first FEOL parameter variable multiplied by the first FEOL correction factor and a first BEOL parameter variable multiplied by the first BEOL correction factor, and

wherein the second model equation comprises the first FEOL parameter variable multiplied by the second FEOL correction factor and the first BEOL parameter variable multiplied by the second BEOL correction factor.

13. The method of Claim 12, wherein the first model equation is given by:

$$D1 = (1 + FCF1*FP1)*(1 + BCF1*BP1)$$

where D1 is the first output delay, FCF1 is the first FEOL correction factor, FP1 is the first FEOL parameter variable, BCF1 is the first BEOL correction factor, and BP1 is the first BEOL parameter variable, and

wherein the second model equation is given by:

$$D2 = (1 + FCF2*FP1)*(1 + BCF2*BP1)$$

where D2 is the second output delay, FCF2 is the second FEOL correction factor, and BCF2 is the second BEOL correction factor.

14. The method of Claim 13, wherein the first FEOL parameter is transistor speed, and wherein the first FEOL correction factor and the second FEOL correction factor are both equal to one.

15. The method of Claim 9, wherein the IC comprises a field programmable gate array (FPGA), and wherein measuring the first measured output delay and the second measured output delay comprises:

configuring the FPGA as a measurement circuit;

reading the first measured output delay from the first embedded test circuit using the measurement circuit; and

reading the second measured output delay from the second embedded test circuit using the measurement circuit.

16. An integrated circuit (IC) chip comprising an IC formed on a substrate, the IC comprising:

a first interconnect layer;

a first embedded test circuit comprising a first ring oscillator coupled to a first test load, the first test load comprising an interconnect structure formed in the first interconnect layer; and

a second embedded test circuit comprising a second ring oscillator, the second ring oscillator comprising an unloaded ring oscillator, and the second ring oscillator being substantially similar to the first ring oscillator.

17. The IC chip of Claim 16, further comprising:

a second interconnect layer; and

a third embedded test circuit comprising a third ring oscillator coupled to a third test load, the third test load comprising an interconnect structure formed in the second interconnect layer, and the third ring oscillator being substantially similar to the first ring oscillator.

18. The IC chip of Claim 16, further comprising a third embedded test circuit, the third embedded test circuit comprising a third ring oscillator,

wherein the first ring oscillator comprises a first transistor type, and

wherein the third ring oscillator comprises a second transistor type.

19. The IC chip of Claim 16, wherein the substrate comprises a wafer, and wherein a plurality of additional ICs is formed on the wafer.

20. The IC chip of Claim 16, wherein the IC comprises a field programmable gate array (FPGA), and wherein the FPGA is configured as a measurement circuit for reading a first output signal from the first embedded test circuit and a second output signal from the second embedded test circuit.

21. A system for analyzing an integrated circuit (IC) comprising:

means for measuring a first delay value from a first embedded test circuit in the IC, the first embedded test circuit comprising a first ring oscillator coupled to a first test load, the first test load representing an interconnect path in the IC;

means for measuring a second delay value from a second embedded test circuit in the IC, wherein the second embedded test circuit is an unloaded test circuit, the second embedded test circuit comprising a second ring oscillator; and

means for comparing the first delay value to the second delay value.

22. The system of claim 21 wherein the IC comprises an FPGA.